We claim:

1. Apparatus for providing port priority functions in a very long instruction word (VLIW) processor comprising:

a register of at least double word width having at least two single word write enables; and

means for resolving a write priority conflict between instructions on a single word basis thereby enabling operation to complete normally on a single word portion of said register of at least double word width that is not in conflict even though at least one other single word portion of said register of at least double word width is in conflict.

2. The apparatus of claim 1 wherein said register of at least double word width has a width of at least 64-bits, the single word is a 32-bit word, a double word is a 64-bit word, and port priorities are defined on the 32-bit word basis to control said write enable signals to a register file containing said register of at least double word width.

3. The apparatus of claim 2 wherein double word and single word data type instructions are mixed within a common very long instruction word (VLIW).

4. The apparatus of claim 1 further comprising port priority logic to control the at least two single word write enables.

5. The apparatus of claim 1 wherein a plurality of said at least double word width registers are contained in a register file which is a compute register file (CRF), an address register file (ARF) or any register file in the processor complex wherein multiple instructions may conflict on subdata types of operations.

6. The apparatus of claim 1 wherein non-conflicting word operations are completed normally while conflicting word operations are prioritized for completion utilizing the port priority logic.

7. The apparatus of claim 6 wherein the port priority logic further comprises:

a plurality of write selection multiplexers for selectably writing a single word to a selected location in said register subject to priority controlled load enable and multiplexer selection signals.

8. The apparatus of claim 7 further comprising:

a plurality of write port address decoders producing output location select signals; and

a plurality of logical OR gates connected to the write port address decoders' output location select signals and producing the priority controlled load enable signals as their outputs.

9. The apparatus of claim 8 further comprising:

a plurality of priority encoders also connected to the write port address decoders' output location select signals to produce write selection multiplexer select signals.

10. The apparatus of claim 5 wherein the port priority logic establishes port priority from highest priority to lowest priority order as follows: memory load ALU, MAU, and DSU operations.

11. The apparatus of claim 1 wherein said means for resolving a write priority conflict comprises port priority logic that is programmable.

12. The apparatus of claim 11 further comprising a load very long instruction word (LVa) instruction employing three priority bits to specify up to eight port priority orderings for a very long instruction word (VLIW) being loaded into VLIW instruction memory (VIM).

13. The apparatus of claim 12 wherein said three priority bits are loaded into VIM and when an execute VLIW (XV) instruction is executed, the port priority bits are read out of the VIM and the port priority logic is setup prior to the VLIW execution cycle.

14. A method for providing port priority functions in a very long instruction word (VLIW) processor comprising:

establishing a register file having registers of at least double word width and having at least two single word write enables; and

resolving a write priority conflict between instructions on a single word basis thereby enabling operation to complete normally on a single word portion of one register of at least double word width that is not in conflict even though at least one other single word portion of said one register of at least double word width is in conflict.

15. The method of claim 14 wherein said at least double word width is defined as 64-bits, the single word is defined as a 32-bit word, and port priorities are defined on the 32-bit word basis to control said write enable signals to a computer register file (CRF) containing the register file.

16. The method of claim 15 further comprising the step of:

mixing double word and single word data type instructions within a common very long instruction word (VLIW).

17. The method of claim 14 further comprising the step of:

utilizing port priority logic to control the at least two single word write enables.

18. The method of claim 17 further comprising the step of:

completing non-conflicting word operations while conflicting word operations are prioritized for completion utilizing the port priority logic.

19. The method of claim 14 further comprising the step of:

utilizing port priority logic that is programmable to resolve the write priority conflict.

20. Apparatus for providing port priority functions in a very long instruction word (VLIW) processor comprising:

a register file having registers of at least single word width and having at least two half-word write enables; and

means for resolving a write priority conflict between instructions on a half-word basis thereby enabling operation to complete normally on a half-word portion of one register of at least single word width that is not in conflict even though at least one other half-word portion of the said one register of at least single word width is in conflict.

21. The apparatus of claim 20 wherein said at least single word width is 32-bits, the half-word is 16-bits, and port priorities are defined on the 16-bit half-word basis to control said write enable signals to a compute register file (CRF) containing said register file.

22. The apparatus of claim 21 wherein single word and half-word data type instructions are mixed within a common very long instruction word (VLIW).

23. The apparatus of claim 20 further comprising port priority logic to control the at least two half-word write enables.

24. The apparatus of claim 20 wherein non-conflicting half-word operations are completed normally while conflicting half-word operations are prioritized for completion utilizing the port priority logic.

25. The apparatus of claim 20 wherein the means for resolving a write priority conflict further comprises:

programmable port priority logic.

26. A method for providing port priority functions in a very long instruction word (VLIW) processor comprising:

establishing a register file having registers of at least single word width and having at least two half word write enables; and

resolving a write priority conflict between instructions on a half-word basis thereby enabling operation to complete normally on a half-word portion of said register of at least single word width that is not in conflict even though at least one other half-word portion of said one register of at least single word width is in conflict.

27. The method of claim 26 wherein said at least single word width is defined as 32-bits, the half-word is defined as 16-bits, and port priorities are defined on the 16-bit half-word basis to control said write enable signals to a compute register file (CRF) containing the register file.

28. The method of claim 27 further comprising the step of:

mixing single word and half-word data type instructions within a common very long instruction word (VLIW).

29. The method of claim 26 further comprising the step of:

utilizing port priority logic to control the at least two half-word write enables.

30. The method of claim 29 further comprising the step of:

completing non-conflicting half-word operations normally while conflicting half-word operations are prioritized for completion utilizing the port priority logic.

31. Apparatus for providing port priority functions in a very long instruction word (VLIW) processor comprising:

a register of at least half-word width having at least two byte write enables; and

means for resolving a write priority conflict between instructions on a byte basis thereby enabling operation to complete normally on a single byte portion of the register of at least half-

word width that is not in conflict even though at least one other single byte portion of the register of at least half-word width is in conflict.

32. The apparatus of claim 31 wherein the at least half-word width is at least 16-bits, the byte is 8 bits, and port priorities are defined on the byte basis to control said write enable signals to a compute register file (CRF).

33. The apparatus of claim 32 wherein half-word and byte data type instructions are mixed within a common very long instruction word (VLIW).

34. The apparatus of claim 31 further comprising port priority logic to control the at least two byte write enables.

35. The apparatus of claim 31 wherein non-conflicting byte operations are completed normally while conflicting byte operations are prioritized for completion utilizing the port priority logic.

36. A method for providing port priority functions in a very long instruction word (VLIW) processor comprising:

establishing a register of at least half-word width having at least two single byte write enables; and

resolving a write priority conflict between instructions on a byte basis thereby enabling operation to complete normally on a single byte portion of the register of at least half-word width that is not in conflict even though at least one other single byte portion of the register of at least half-word width is in conflict.

37. The method of claim 36 wherein the at least half-word width is defined as at least 16-bits, the byte is defined as 8-bits, and port priorities are defined on the byte basis to control said write enable signals to a compute register file (CRF).

38. The method of claim 37 further comprising mixing half-word and byte data type instructions within a common very long instruction word (VLIW).

39. The method of claim 36 further comprising utilizing port priority logic to control the at least two single byte write enables.

40. The method of claim 39 comprising the steps of:

completing non-conflicting byte operations normally while conflicting byte operations are prioritized for completion utilizing the port priority logic.

41. Apparatus for providing port priority functions in a multiple issue processor comprising:

a register file of width x having y write enables; and

means for resolving a write priority conflict between instructions on a sub-x-width operation thereby enabling a sub-x-width operation to complete normally on the sub-x-width portions of the x-width register that are not in conflict even though at least one other sub-x-width portion of the x-width register file are in conflict.

42. The apparatus of claim 41 wherein the width x is 64-bits, the number of write enables y is eight, the sub-x-width operation is at least one or a multiple number of 8-bit bytes and the port priorities are defined on a byte basis to control said write enable signals to a register file.

43. The apparatus of claim 42 wherein multiple instructions of differing data-type operations are mixed when issued for concurrent execution.

44. The apparatus of claim 41 further comprising port priority logic to control the y write enable signals for the portions of the x-width register that are in conflict.

45. The apparatus of claim 41 wherein the non-conflicting sub-x-width operations are completed normally while the conflicting sub-x-width operations are prioritized for completion utilizing the port priority logic.

46. The apparatus of claim 41 wherein said means for resolving a write priority conflict comprises port priority logic that is programmable.